Digital Test Technology

Course Information

The Digital Test Technology Course is designed to provide a foundation of knowledge that is fundamental to all aspects of semiconductor test engineering.

In order to meet the testing challenges of modern VLSI circuits, digital component test has made significant advances over the past few years. In addition to the tried and true test methodologies of the past, engineers must now understand topics such as Defect Oriented Testing, Fault Coverage, Design-for-Testability, IDDQ and Structural Test. These topics have moved from the "experimental" phase into mainstream test and are now introduced in this course.

The Course

Lecture begins with an overview of the Semiconductor and ATE industry. ATE system architecture and functionality are explained along with the terminology used to describe semiconductor testing. Interpreting device specifications is emphasized and discussed with each test procedure. DC, AC and Functional tests are explained in detail and various test methods are discussed along with the advantage and disadvantage of each method.

Device characterization, yield analysis, debug techniques, datalogs and shmoo plots are also explained. Proper programming practices that minimize test times, insure test integrity and produce safe, reliable test sequences are taught throughout.

Who Should Attend

Test and Product Engineers, Engineering Managers, Sales Engineers, Field Service Engineers and Maintenance Technicians have all benefited from this course – it is recommended as a starting point for all engineers both digital and mixed signal.

When & Where

Soft Test offers training services at our Sunnyvale CA facility on a regular basis and we also offer on site training at your facility. Give us a call for additional information and class schedules or visit our web site at **www.soft-test.com**

The Cost

Tuition is $1,500 per attendee and includes all course material including the *Fundamentals of Digital Semiconductor Testing* text. Contact Soft Test for on site pricing.

Class Registration

Registration forms are available on our web site or contact our East Coast office at 386.478.1979. Email inquires to **admin@soft-test.com**

Summary

Test engineering is typically learned *on the job* by paring a junior engineer with a more experienced colleague. This consumes valuable resources and slows progress, but there is a better way. Now you can jump start your educational process and receive what has typically taken years of on the job training in just one week.

There's More

Please visit our web site at www.soft-test.com for additional information on this course. Soft Test also offers technical training and publications for Mixed Signal Test, Memory Test and a variety of subjects related to the semiconductor industry.

Digital Test Technology

Course Content

Course Length: 5 days

Purpose

This course is designed to explain the concepts and techniques used in testing digital semiconductors with ATE equipment. Practical information is presented pertaining to test program development, debugging techniques and yield analysis. DC, AC, Functional and Device Characterization are discussed in detail. An overview of current test requirements of semiconductor industry is also presented.

Our Goal

Our goal is to provide useful, practical information that will quickly improve the skill set required to be a productive Test or Product Engineer. We present an environment where questions and interactions are welcome and everyone is treated with respect regardless of their experience level.

Content

The course information presented includes the following:

- ATE system architecture and functionality
- A solid understanding of device specifications
- An understanding of how and why each DC, AC and Functional test is performed
- Understanding program flow and the trade-off of data collection vs. test time
- Interpreting datalogs, characterization data and shmoo plots
- Methods for developing trouble-shooting and diagnostic skills
- Introduction to DFT, BIST, Scan, Structural and Defect Oriented Testing
- Methods for improving the quality of test programs
- Techniques to increase productivity for test and product engineers

Distribution Materials

The *Fundamentals of Digital Semiconductor Testing* text and all classroom materials are provided with the course

Prerequisites

An understanding of elementary electronics and a desire to learn

Digital Test Technology
Course Syllabus

Pre-Test Evaluation

Introduction to Test
Basic Terms
Why Test?
What is The Correct Way to Test?
What will be Tested?
The Test System
The PMU
Device Power Supplies (DPS)
The Pin Electronics
Basic Guidelines of Test Engineering
Chapter Questions — Review

Test System Architecture
Basic Terms
The Test System
What's in a Test System?
Control Functions
DC Instrumentation
Functional/AC Instrumentation
Mechanical
Software
Basic Guidelines of Test Engineering
Chapter Quiz - Review

Device Specifications
Basic Terms
The Device Specifications
Test Conditions and Limits
Parameters that Apply to DC Parametric Testing
Parameters that Apply to Functional and AC Testing
Logical Functions
Reading Device Specifications
256 x 4 RAM Specifications
Interpreting the Device Specification
Device Specifications and Test Conditions
Chapter Questions — Review

Opens and Shorts - PMU Method
Why Test for Opens and Shorts?
Opens and Shorts Serial Static Method
Chapter Questions — Review

Verifying DC Parameters
Basic Terms
Binning

Program Flow
Test Summary
Traceability
DC Tests and the Hidden Resistance
Ohm’s Law and DC Testing
VOH/IOH
VOL/
IDD Gross Current
IDD Static Current
IDDQ Current
IDD Dynamic Current
Input Currents (IIL/IIH)
Resistive Inputs—Pull–ups and Pull–downs
Output Fanout
High Impedance Currents (IOZL/IOZH)
Input Clamp (VI)
Output Short Circuit Current (IOS)
Chapter Questions — Review

Verifying Functional Parameters

Introduction to Functional Testing
Basic Terms
Functional Testing
The Test Cycle
Input Data
Input Signal Formats
Developing Input Signal Timings
Output Data
Testing Outputs
Testing Valid (L/H) Output Levels
Output Testing using an Edge Strobe
Output Testing using a Window Strobe
Testing High Impedance (Z-state) Output Levels
Output Current Loading
Developing Output Strobe Timing
Output Loading for AC Tests
Vector Data
Functional Specifications
Gross Functional Tests
Equation Based Timing
Functionally Testing a Device
Sample Device Specification
Specification Test Conditions for the Clocked Inverter
Gross Functional Test Conditions for the Clocked Inverter
Test Program Statements for Clocked Inverter
Standard Functional Tests
Opens and Shorts - Functional Method
VIL/VIH
VOL/IOL VOH/IOH Functional Test
Resistive Output Loading Input/Output Levels
Functional Z–State — High Impedance Testing
Open Drain / Open Source
Chapter Questions — Review

Testing AC Parameters

AC Parametric Testing
Read & Record
Go–Nogo Testing
Compromises
Standard AC Parameters
Rise Time / Fall Time
Setup Time
Hold Time
Propagation Delay Measurements
Minimum Pulse
Maximum Frequency
Output Enable Time
Output Disable Time
AC Specifications from 256 x 4 Static RAM Data Sheet
Developing Functional Timing
Write Cycle Timing Student Exercise
Chapter Questions — Review

Device Characterization

Characterization Overview
Test Vectors and Characterization
Defining Characterization Parameters
Common Characterization Parameters
Use of Test System Tools
The Test System Datalogger
The Linear
The Binary Search
Binary Search - Input Timings
Binary Search - Output
Threshold/Level Search
Shmoo Plots
Chapter Questions — Review

Design for Testability

Design For Testability and Functional Testing
Fault Models
Fault Coverage
Stuck-At Fault Analysis
What is DFT?
Scan Design
Boundary Scan IEEE 1149.1
Boundary Scan Architecture
Boundary Scan Register Functions
Boundary Scan Register Logic
BIST
DFT Considerations
Chapter Quiz - Review

Course Summary

Post-Test Evaluation

Digital Test Technology

Knowledge Evaluation 2009

If you miss more than 3, you are a good candidate for the Digital Test Technology class.

Name: ________________________________ Date: _________________________

Match the terms with the definitions below.

A: Negative	F: Preconditioning	K: Boundary Scan	P: VOL	U: Fault Coverage
B: Static	G: Dynamic	L: Setup Time	Q: IOL	V: DPM
C: VREF or VCOM	H: VIL	M: Pin Electronics	R: VDDMAX	W: Fault
D: IDD or ICC	I: Binning	N: Comparators	S: Positive	X: DFT
E: IOH	J: Hold Time	O: Wafer Test	T: Defect	Y: Bi-directional or IO

_______ 1) The parameter that defines the acceptable power supply current of a semiconductor device.

_______ 2) This term indicates that the device under test is actively changing logic states.

_______ 3) The AC parameter that defines the minimum amount of time that data must be held after a reference signal reaches a certain voltage point.

_______ 4) A device pin that functions as an input, an output and is also capable of achieving a high impedance state.

_______ 5) A term used to describe logic that is added to a circuit design to improve its testability.

_______ 6) A means of categorizing or sorting tested devices into their appropriate groupings.

_______ 7) The parameter that defines the minimum current that an output must source when driving a logic one.

_______ 8) Circuitry located in the test head used to supply input signals to the device under test and to receive output signals from the device under test.

_______ 9) The reference voltage associated with the dynamic current loads, used to control the switching point of IOL and IOH currents.

_______ 10) The parameter that defines the maximum voltage which may be applied to an input pin when applying a logic zero.

_______ 11) A physical flaw introduced into a circuit during the manufacturing process.

_______ 12) The polarity of current when flowing into the test system.

_______ 13) A measure of the effectiveness of a vector test pattern.

_______ 14) The polarity of current supplied by the test system during an IOL test.

_______ 15) The name of the IEEE 1149.1 standard

Select the correct answer for the questions below.

16) The VIL/VIH specifications are verified by executing:
a. A DC test
b. A functional test
c. Only verified through Failure Analysis
d. No test, these parameters are guaranteed by design

17) Propagation measurements are only made at outputs:
a. True
b. False

18) When performing a functional opens and shorts test, the current is forced by:
a. The PMU
b. The programmable current loads
c. Voltage is normally forced, not current
d. None of the above

19) A linear search typically executes slower than a binary search
a. True
b. False

20) When Performing the VOH test, the current forced during the test is:
a. A positive current
b. A negative current
c. a or b

21) The IIL/IIH test verifies:
a. Input capacitance
b. Input threshold levels
c. Input impedance

22) When the device specifications defines VDD as 3.0V +/- 5%, the value of VDDMIN is:
a. 3.15 volts
b. 3.25olts
c. 2.85 volts
d. It depends on the technology

23) Open drain outputs do not have the ability to:
a. Drive a logic 0
b. Drive a logic 1
c. Source current
d. B and C

24) The output enable parameter tests the transition time of an output changing from driving valid logic levels to a high impedance state.
a. True
b. False

25) The first testing to take place on a new circuit design is often called:
a. Quality Assurance Test
b. Design Validation
c. Class Test
d. Incoming Inspection

To check your answers please visit our web site at
`http://www.soft-test.com/digital/answers.htm`